IFW 2811

Docket:
90065.99R272/17732.6323

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jifa Hao, et al.	)	
		)	Examiner:
Serial No.:	09/654,845	)	Ori Nadav
		)	
Filed:	September 1, 2000	)	Art Unit:
		)	2811
Title:	POWER SEMICONDUCTOR DEVICE WITH HIGH AVALANCHE CAPABILITY AND PROCESS FOR FORMING SAME	)	

AMENDMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA22313-1450

Dear Sir:

In response to the office action mailed February 13, 2004, please consider the following remarks.

All of the claims are rejected under 35 USC Section 103(a) based on a combination of two or more references. In these remarks the Applicants will demonstrate that the references do not show or suggest the limitations of the claims and that the invention as claimed provides results that are unexpected. Evidence of these results is found in the specification and the Manual of Patent Examining Procedure requires that this comparative evidence be considered:

> Examiners must consider comparative data in the specification which is intended to illustrate the claimed invention in reaching a conclusion with regard to the obviousness of the claims. *In re Margolis, 785* F.2d 1029,228 USPQ 940 (Fed.Cir.1986). The lack of objective evidence of nonobviousness does not weigh in favor of obviousness. *Miles Labs.Inc.v.Shandon Inc.*, 997 F.2d 870, 878, 27 USPQ2d 1123, 1129 (Fed.Cir.1993), *cert.denied,* 127 L.Ed. 232 (1994). However, where a *prima facie* case of obviousness is established, the failure to provide rebuttal evidence is dispositive. MPEP 716.01(a)

The Specification on page 5, TABLE 1, compares identical N+, N-, P-, P+ structures made with the invention (sample) and without the invention (control). The results show dramatic differences between the amount of UIS energy that is withstood by the samples with the invention and the controls without the invention. For all of the examples given, the improvement is at least one order of magnitude. This dramatic improvement is likely due to the reduced platinum concentration, the location of the recombination centers in substantially the P- and N- layers, and the reduced thickness of the P- layer. By reducing the diffusion temperature by about one or two percent (940°C for samples; 950°C for controls), the UIS energy performance of the device was improved by over 1500 percent for the Samples 1 and 2. Sample 3 had a UIS of 72 mJ compared to the control that had virtually no UIS capability. In all examples the improvement in UIS performance left other key parameters unaffected. In other words, the invention had no material adverse impact on the forward voltage (VF), transient reverse recovery time (TRR) and reverse blocking voltage (BVR) when compared to the corresponding parameters of the control devices.

The invention has certain structural characteristics that are unique. It has P+ and P- layers whose combined thickness is between 5 -12 microns. In addition, the recombination centers for the noble metal impurities are substantially in the N- and P- layers. These limitations emphasize the relative thinness of the P type layers combined with the requirement that the noble dopants in the device are substantially disposed in the N- and P- layers. The lower diffusion temperature in the process keeps the noble impurities substantially in the N- and P-layers. Applicants believe that limiting the diffusion of the noble dopants to substantially the N- and P-layers accounts for the improved UIS characteristic of the invention. Moreover, the art of record fails to show or suggest these particular limitations that are characteristic of the invention that has dramatically improved UIS characteristics.

Certain findings in the office action are not supported by the references. For example, the office action found that Torkura et al. (5545908) teaches "a power semiconductor device having high avalanche capability." The reference is silent about it avalanche capability. A key word search of the text of the reference fails to show or suggest any occurrence of the word "avalanche." Thus, there is no basis for this finding and it must be withdrawn.

That finding is reasserted on pager 5 of the action where the Examiner wrote that high avalanche capability is inherent in prior art devices that comprise recombination centers because "avalanche capability is a function of the recombination centers."

Applicants traverse this finding of inherency. A review of the references shows no relationship between avalanche and recombination centers. Avalanche is a phenomenon that occurs when high voltage is applied across a power device. In contrast, recombination occurs when a non-equilibrium force, such as voltage or temperature, is removed and the carriers are allowed to recombine. If the Examiner persists in this finding, then Applicants requests that the Examiner provide a reference that teaches the alleged inherent relationship or withdraw the finding. In addition, the finding made by the Examiner implies that more recombination centers improve performance. However, the data in TABLE 1 show that reducing the concentration of platinum results in an increase in UIS performance, so long as the recombination centers are substantially in the P- and N- regions. No reference shows or suggests that claimed relationship.

As stated on page 4 of the Specification, UIS is a measure of avalanche energy that can be dissipated in a device. Only Applicants teache a relationship between UIS/avalanche and recombination centers and thickness of layers. The prior art fails to show or suggest disposing the lower concentration of recombination centers in the central layers of the device (substantially in the P- and N- layers) together with relatively thin P+ and P- layers.

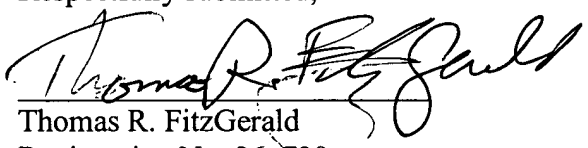
While it is true that other devices have shrunk in size, the Examiner, as one skilled in the art, knows that not every design may be shrunk without modification. All designs include assumptions about how a device works **at a given size**. But shrinking a design may uncover problems that were masked by the larger size design. For example, today the semiconductor industry is nearing the limit for using visible light to form the smallest devices. As device size shrinks, the wavelength of light used to expose photoresist is comparable to the spacing between device features in the photomask. This causes diffraction and interferes with forming an image.

When power semiconductors designs shrink, the smaller designs also encounter scaling problems. Indeed, it is the very invention proposed by the Applicants that permits the further

reduction in size of the devices. The invention enables the substitution of smaller size die to achieve UIS performance comparable to that of a larger conventional die. See TABLE 1. Note that Sample 3 has a UIS of 72 mJ but is only 60 mil^2. It could be substituted for Control 1 that has a die size of 160 mil^2. That is more than a 60% reduction in size for more than a three fold increase in UIS performance. No reference shows or suggests achieving such a dramatic size reduction while keeping its performance features.

In summary, the comparative data presented in the application shows that prior art devices made using conventional process steps result in relatively large size power devices with low UIS capability. However, when devices are modified to have the invention, they are smaller and their UIS capability improves by an order of magnitude.

Respectfully submitted,



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I hereby certify that this **Amendment (4 pages)**
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